2024 EOS/ESD Symposium

Toward a Trillion Transistors
ESD Perspectives on Emerging IC Technologies

Marko Simicic

29 October 2024

Marko Simicic

Works at IMEC

Employment location Leuven

imec
Full-time · 7 yrs 2 mos

- **R&D Team Lead**
  Aug 2024 - Present · 3 mos
  Leuven, Flemish Region, Belgium
- **Principal Member of Technical Staff**
  Jul 2024 - Present · 4 mos
  Leuven, Flemish Region, Belgium
- **R&D Engineer**
  Sep 2017 - Jul 2024 · 6 yrs 11 mos
  Kapeldreef 75, 3001 Leuven, Belgium

2012

REPUBLIKA HRVATSKA
SVEUČILIŠTE U ZAGREBU
FAKULTET ELEKTROTEHNIKE I RAČUNARSTVA

DIPLOMA

Sveučilište u Zagrebu

MARKO SIMIČIĆ

FAKULTET ELEKTROTEHNIKE I RAČUNARSTVA

MAGISTAR INŽENJER
ELEKTROTEHNIKE I
INFORMACIJSKE TEHNOLOGIJE

2018

KU LEUVEN

Marko Simicic

Doctor of Engineering Science (PhD)

Electrical Engineering

imec

5,500 employees from more than 100 nationalities

System partners

Materials partners

Fabless/FABlite/EDA

over 600 partners

Equipment supliers

IDMs/Foundries

Design houses

~12,000 m^2 cleanroom

over 250 tools

Global collaboration with >200 universities

Long-term research pipeline and fundamental insights

Turning academic insights into industrial innovations

imec

2025 International ESD Workshop (IEW)

Announcement and call for posters

Monday 12 May – Friday 16 May 2025

Hotel Dubrovnik, Gajeva ulica 1, Zagreb, Croatia

Abstract Submission

18 November 2024

www.esda.org/events/2025-international-esd-workshop-iew-europe

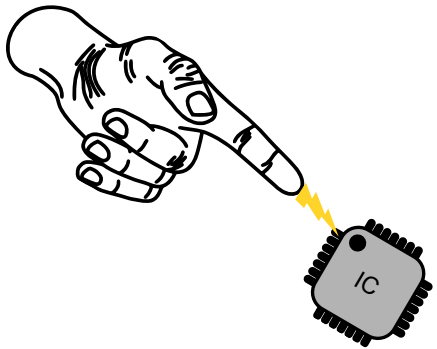
ESD ASSOCIATION®

ElectroStatic Discharge (ESD)

A sudden flow of electricity between two electrically charged objects

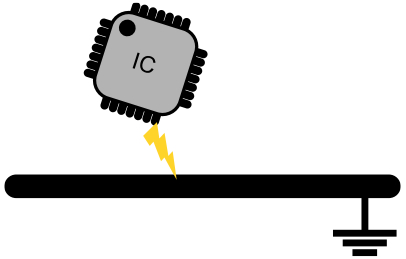
A person touches a device

Human Body Model (HBM)



A device touches a conductor

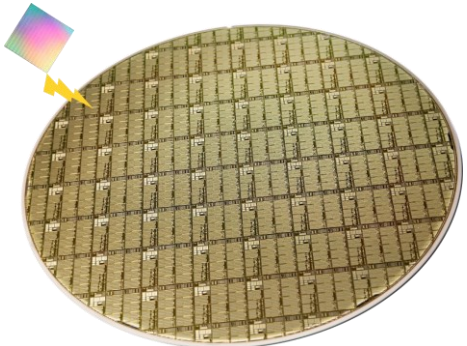
Charged Device Model (CDM)



What about chiplets?

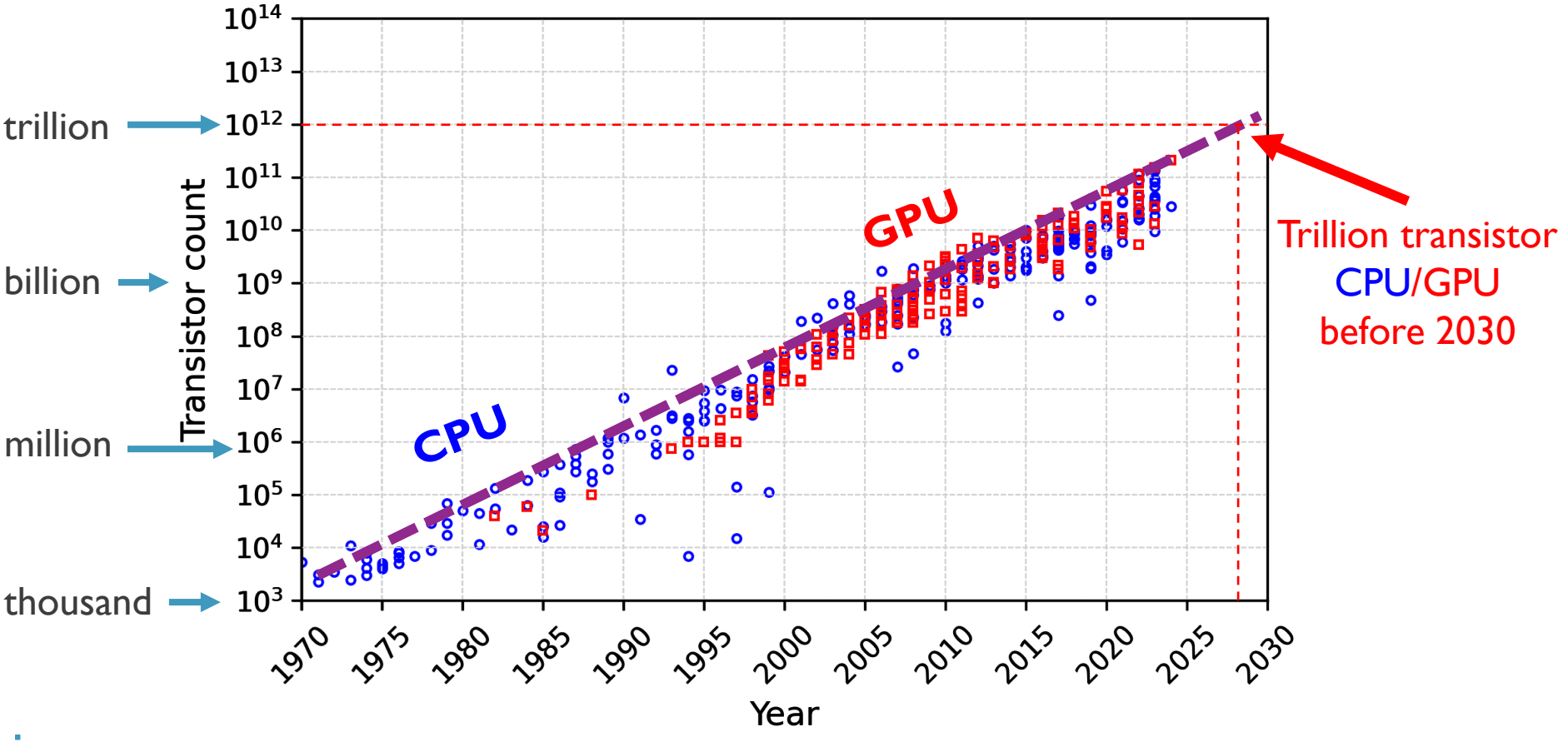
No standard yet, but...

Charged Chiplet Model ? (CCM)



imec

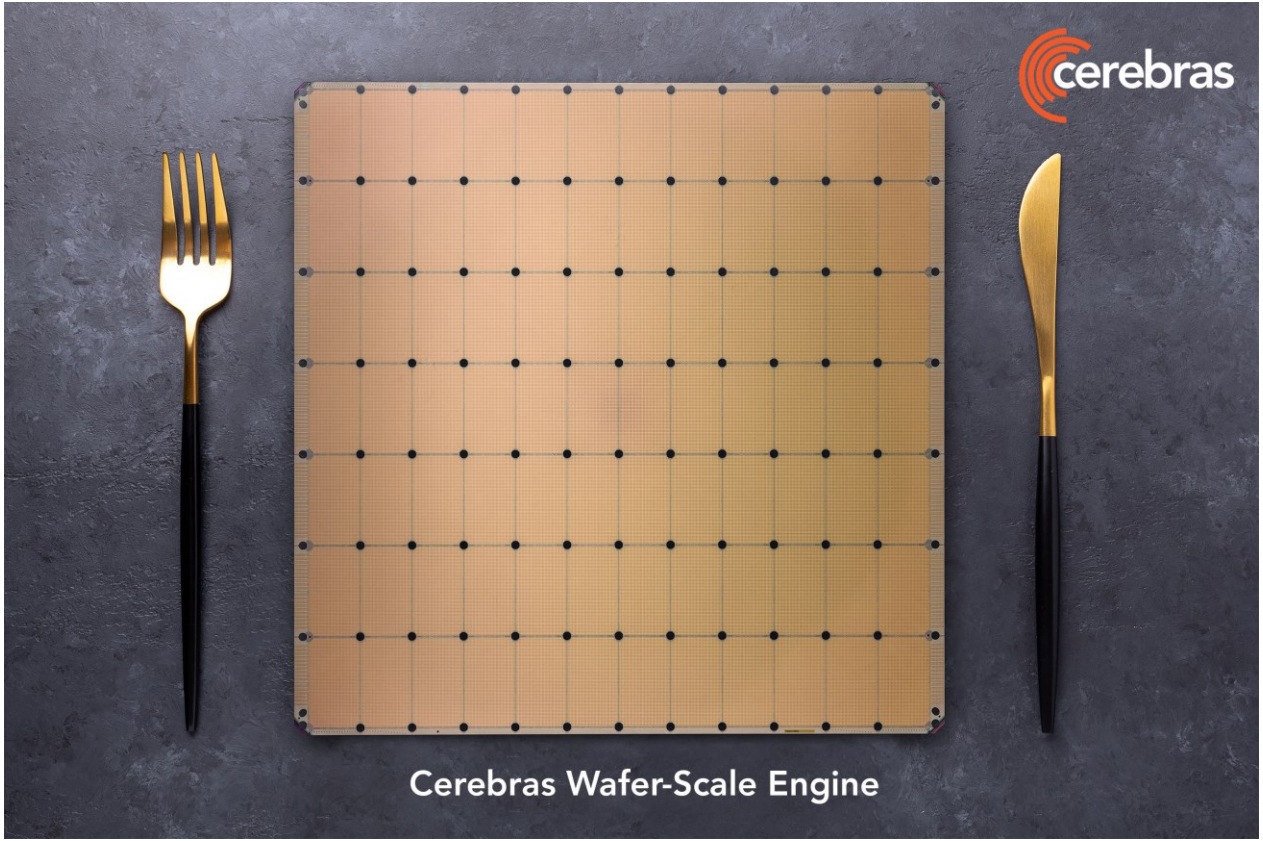
Every semiconductor presentation has to start with... Moore's Law



imec

Except... Cerebras – 4 trillion transistors – August 2024

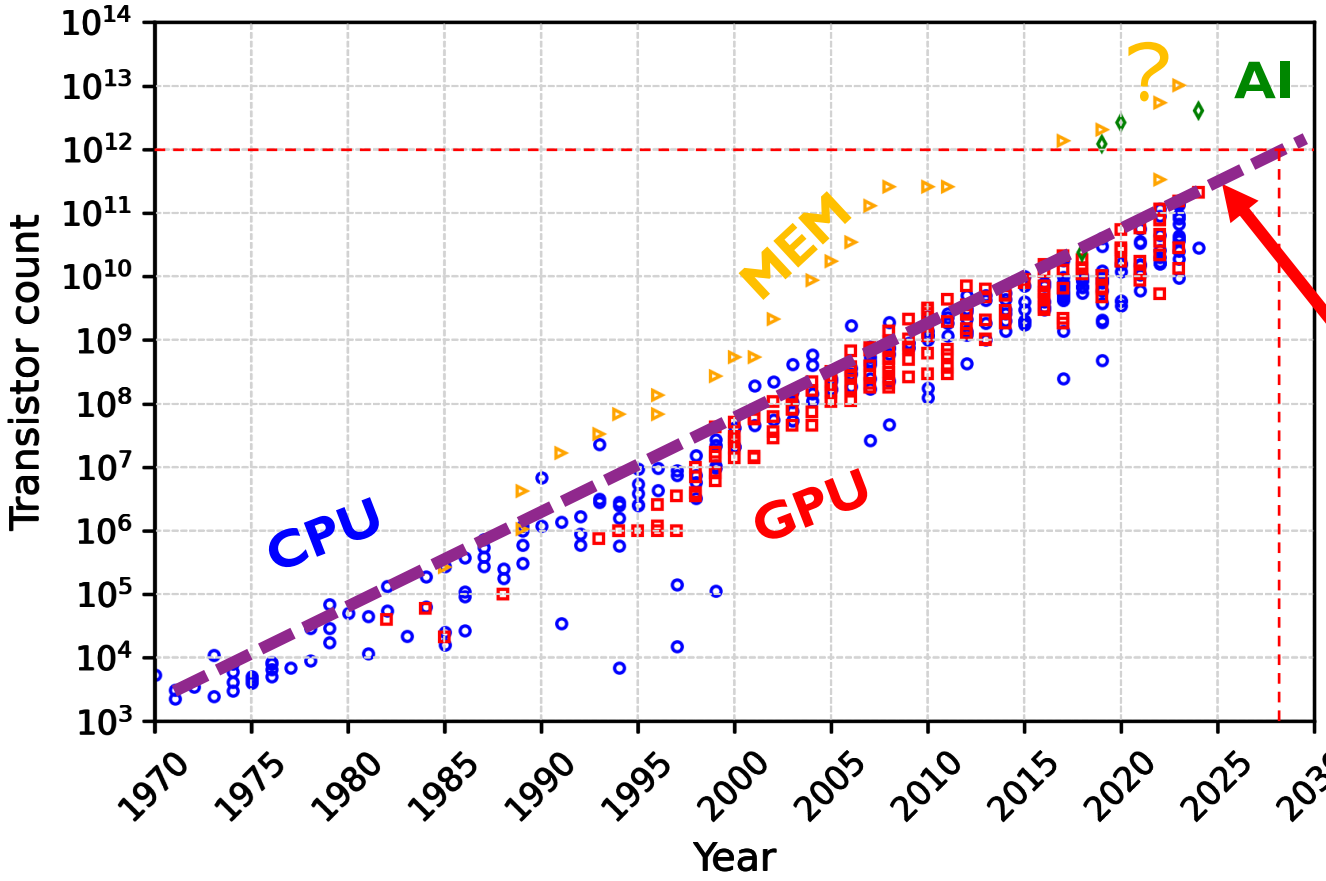
- 3rd generation Wafer Scale Engine
- 46 225 mm^2
- 900 000 compute cores
- 44 GB on-chip memory
- TSMC 5nm technology



"Cerebras Systems Unveils the Industry's First Trillion Transistor Chip", https://www.cerebras.net/press-release/cerebras-systems-unveils-the-industrys-first-trillion-transistor-chip/, accessed 18 August 2024

imec

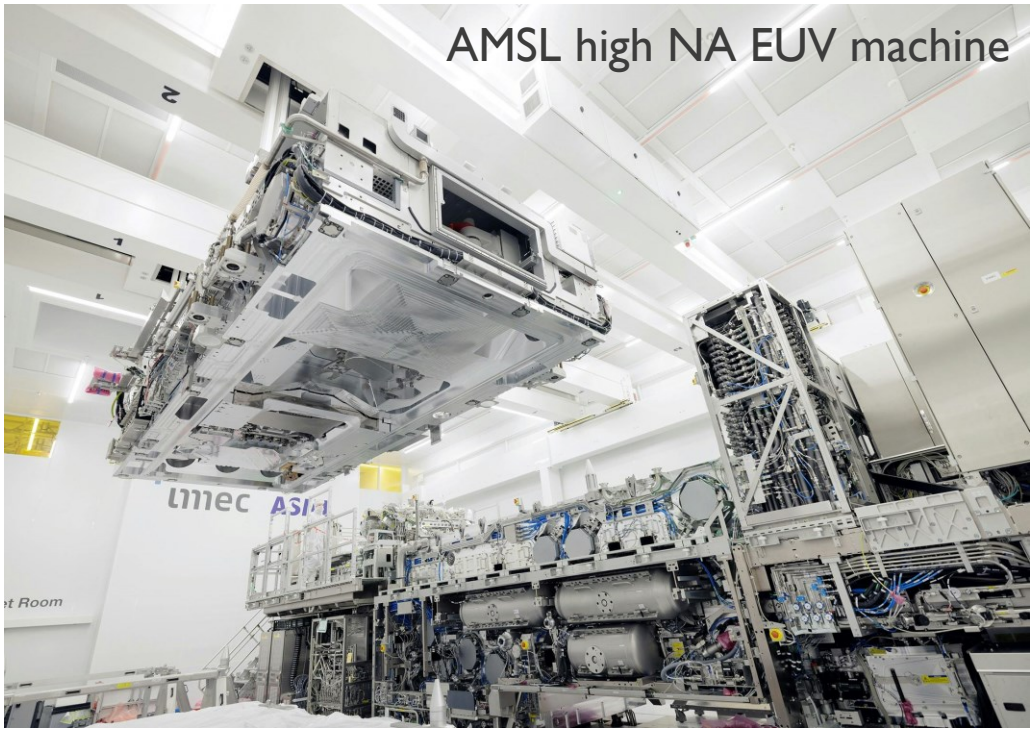
Memory and some AI cores are beyond Moore's scaling

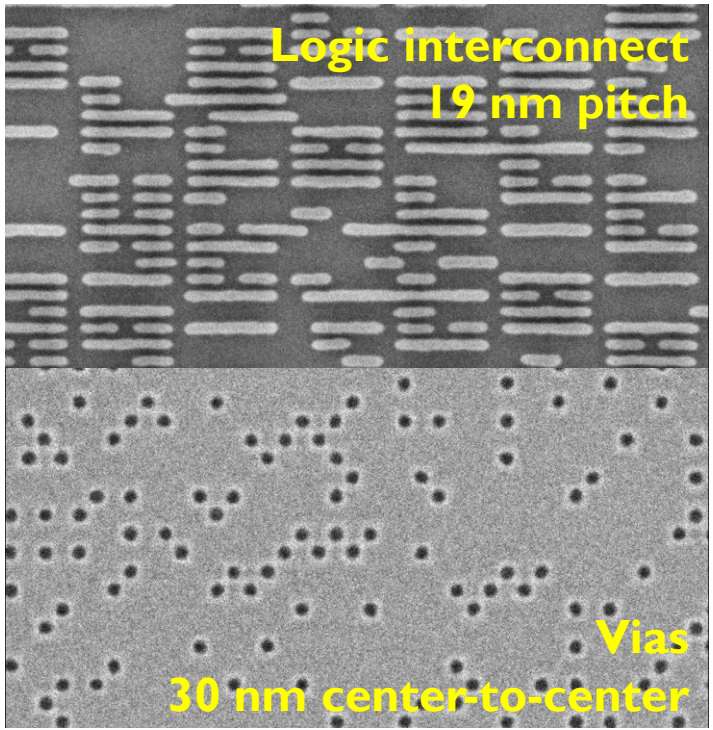


How will this continue?

What can we expect?

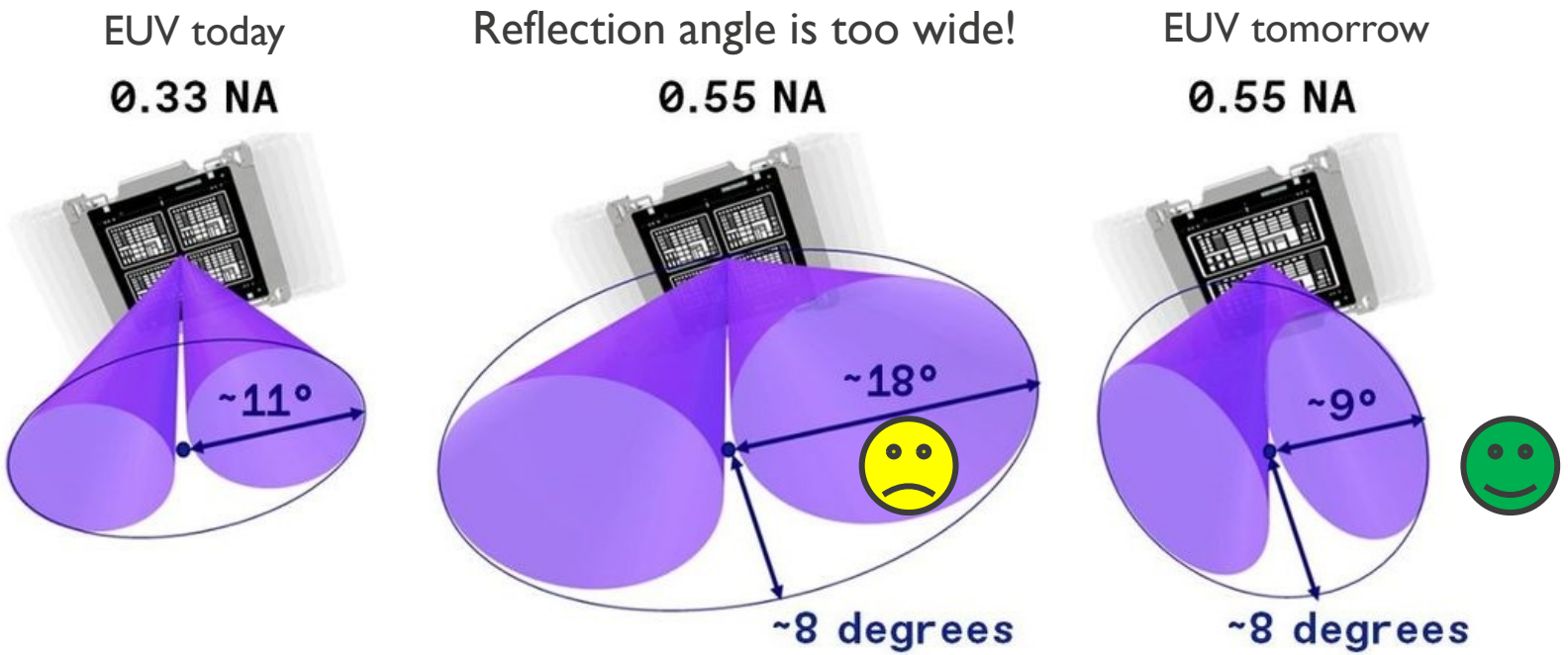
High Numerical Aperture (NA) Extreme-UV (EUV) Lithography





- Imec press release, "Imec and ASML open joint High NA EUV Lithography Lab offering an early development platform to the leading-edge semiconductor ecosystem", 3 June 2024, https://www.imec-int.com/en/press/asml-and-imec-open-joint-high-na-euv-lithography-lab-offering-early-development-platform, accessed: 18 August 2024.
- Imec press release, "Imec demonstrates logic and DRAM structures using High NA EUV Lithography", 7 August 2024, https://www.imec-int.com/en/press/asml-and-imec-open-joint-high-na-euv-lithography-lab-offering-early-development-platform, accessed: 18 August 2024.

Lithography field (reticle) size limits the number of transistors on a monolithic die



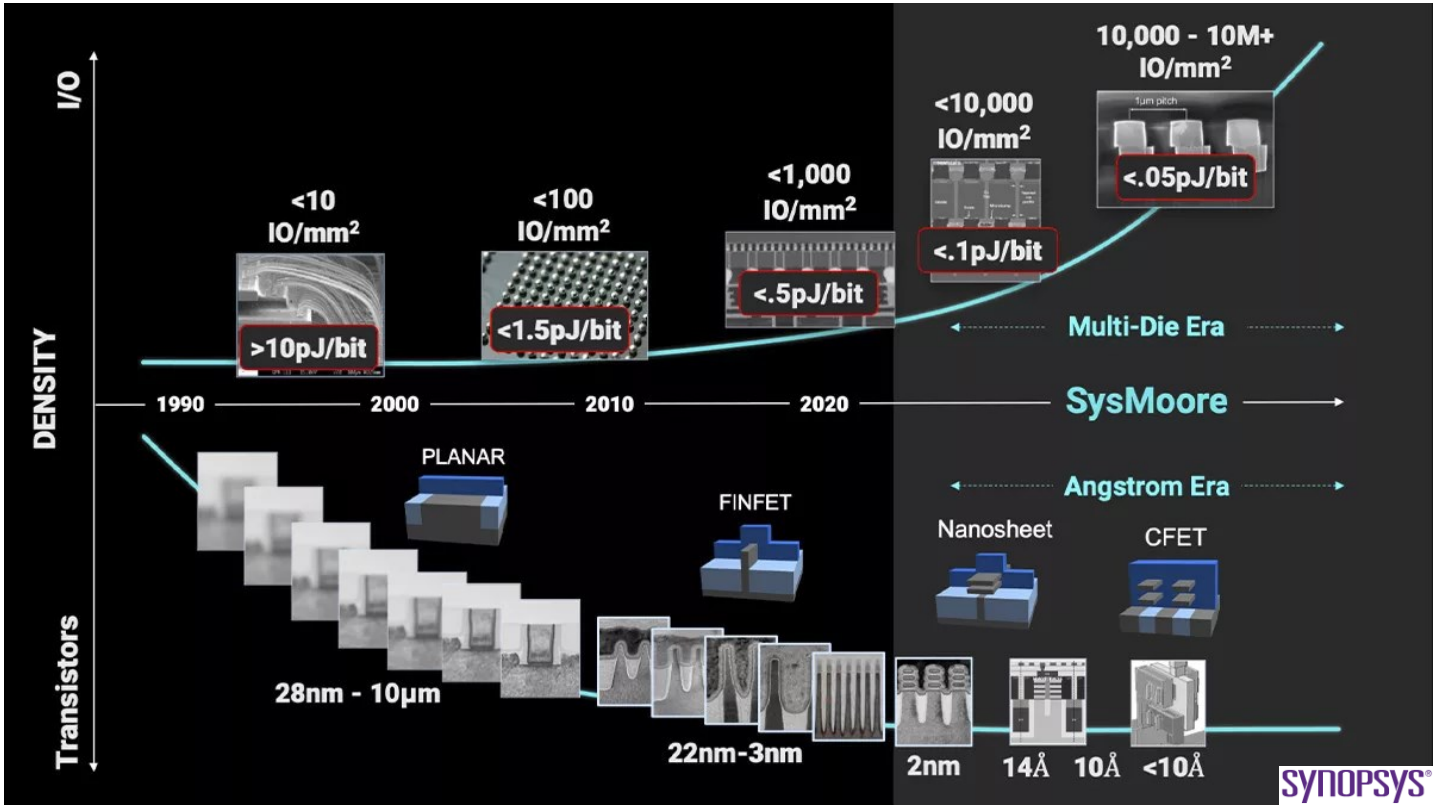
EUV today
Field size: 26 x 33 mm
Maximum single-exposure monolithic chip **size: 858 mm²**

EUV tomorrow
Field size: 26 x 16.5 mm
Maximum single-exposure monolithic **chip size: 429 mm²**

Jan van Schoot, "This Machine Could Keep Moore's Law on Track", IEEE Spectrum, 2023, https://spectrum.ieee.org/high-na-euv, accessed 18 August 2024

imec

Multi-die (chiplet) systems will continue Moore's law



Aart de Geus, "Chapter 1: SysMoore – Systemic Complexity with a Moore's Law Ambition!", https://www.synopsys.com/multi-die-system/how-multi-die-systems-will-change-semiconductor-design.html, accessed 20/10/2023

Logic device roadmap

Logic Scaling Roadmap

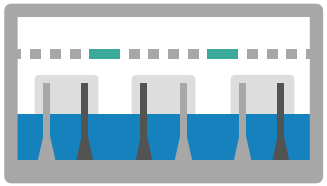
Standard cell evolution enabled by new device architectures

3nm
PP:44-48, MP: 21-24

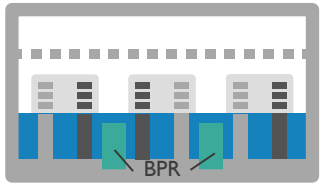
2nm
PP:40-44, MP: 18-21

1.5nm
PP: 40-44, MP: 18-21

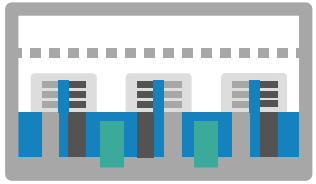
1nm and beyond
PP: 38-42, MP: 15-18



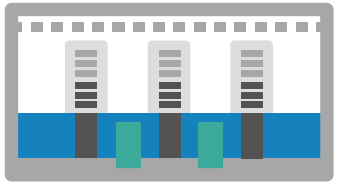
FinFET
5T



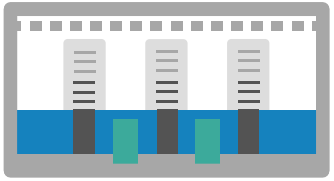
Nanosheets, BPR
5T



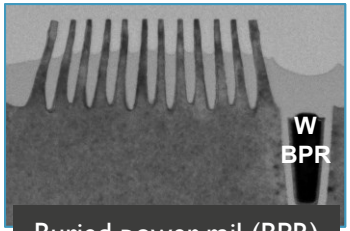
Forksheets, VHV std cell arch.
<5T



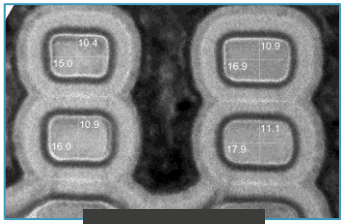
CFET, BEOL w/ airgaps
4T



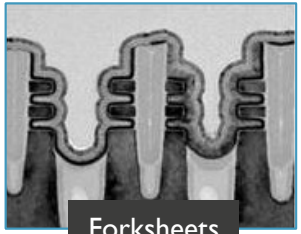
2D atomic channels
<4T



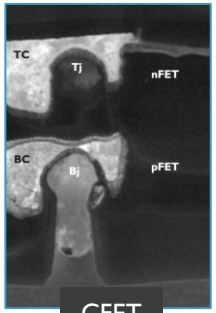
Buried power rail (BPR)



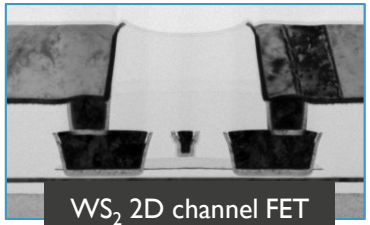
Nanosheets



Forksheets



CFET

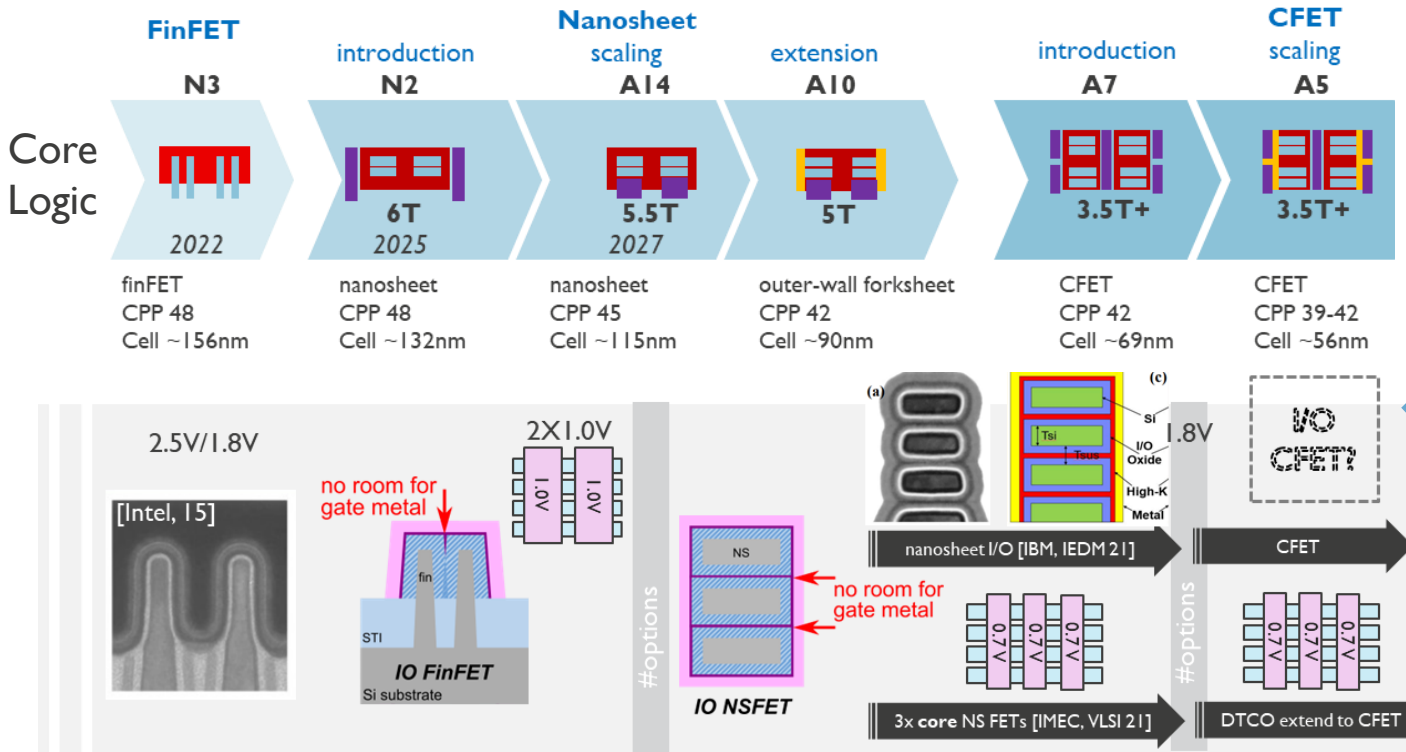


WS_2 2D channel FET

PP: poly pitch (nm)
MP: dense metal pitch (nm)

VHV: Vertical-Horizontal-Vertical **CFET**: Complementary FET

Thick-oxide transistors more challenging in new technologies



Thick-oxide I/Os

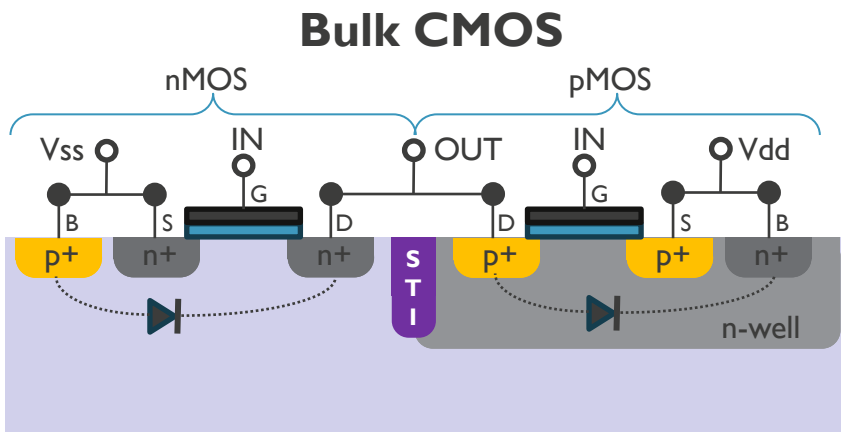
- 2...3xVDD simple inverter

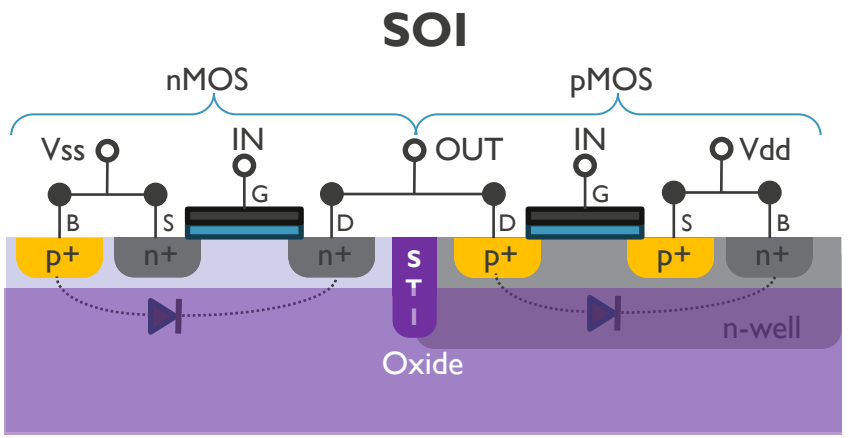
Core-transistor I/Os

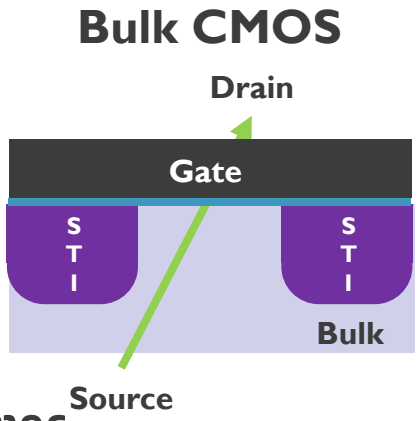
- 2...3xVDD I/O made of stacked core transistors

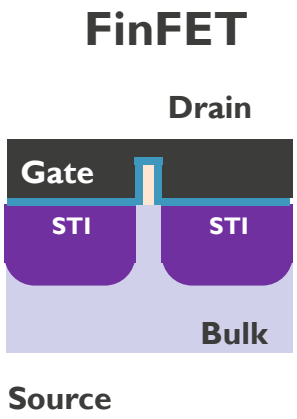
Wen-Chieh Chen et al., "A 1.8V GPIO with Design-Technology-Reliability Co-Optimization in Sub-3nm GAA-NS Technology", JSSC, 2024. **[CFET]**: J. Ryckaert *et al.*, "The Complementary FET (CFET) for CMOS scaling beyond N3," in *2018 IEEE Symposium on VLSI Technology*. doi: 10.1109/VLSIT.2018.8510618. **[intel 15]** - C.-H. Jan et al., "A 14 nm SoC platform technology featuring 2nd generation Tri-Gate transistors, 70 nm gate pitch, 52 nm metal pitch, and 0.0499 um2 SRAM cells, optimized for low power, high performance and high density SoC products," 2015 VLSI Symposium **[imec VLSI 21]** - Hellings, Geert, et al. "Si/SiGe superlattice I/O FinFETs in a vertically-stacked gate-all-around horizontal nanowire technology." 2018 VLSI Symposium, 2018. **[IBM, IEDM 21]** - Bhuiyan, Maruf, et al. "Gate-Last I/O transistors based on stacked gate-all-around nanosheet architecture for advanced logic technologies." 2021 IEDM, 2021.

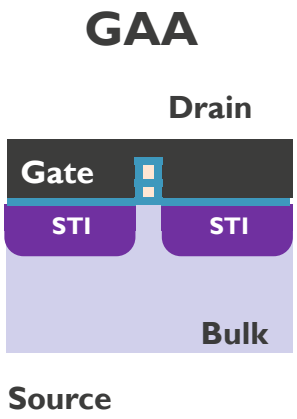
Si bulk is disappearing – FET self-protection is reducing

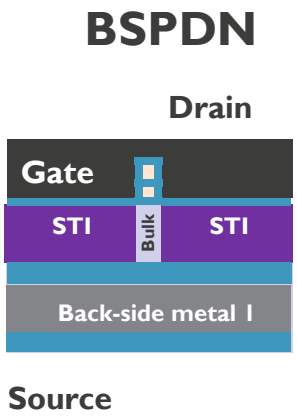








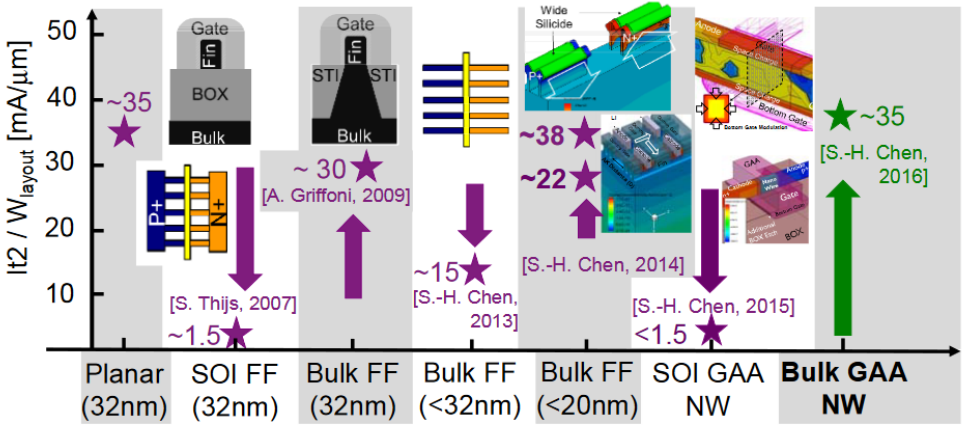




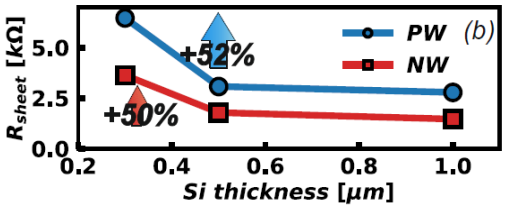
No bulk, but functional backside!

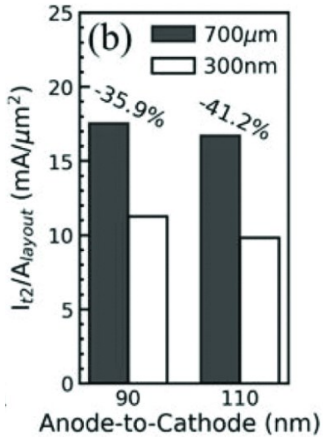
Diode performance is not improving
Planar technologies are better for ESD protection

- Technologies scale
- Diode ESD performance does not scale up



- BSPDN and wafer thinning
- Diode performance is reduced





- Increased resistance = lower ESD performance

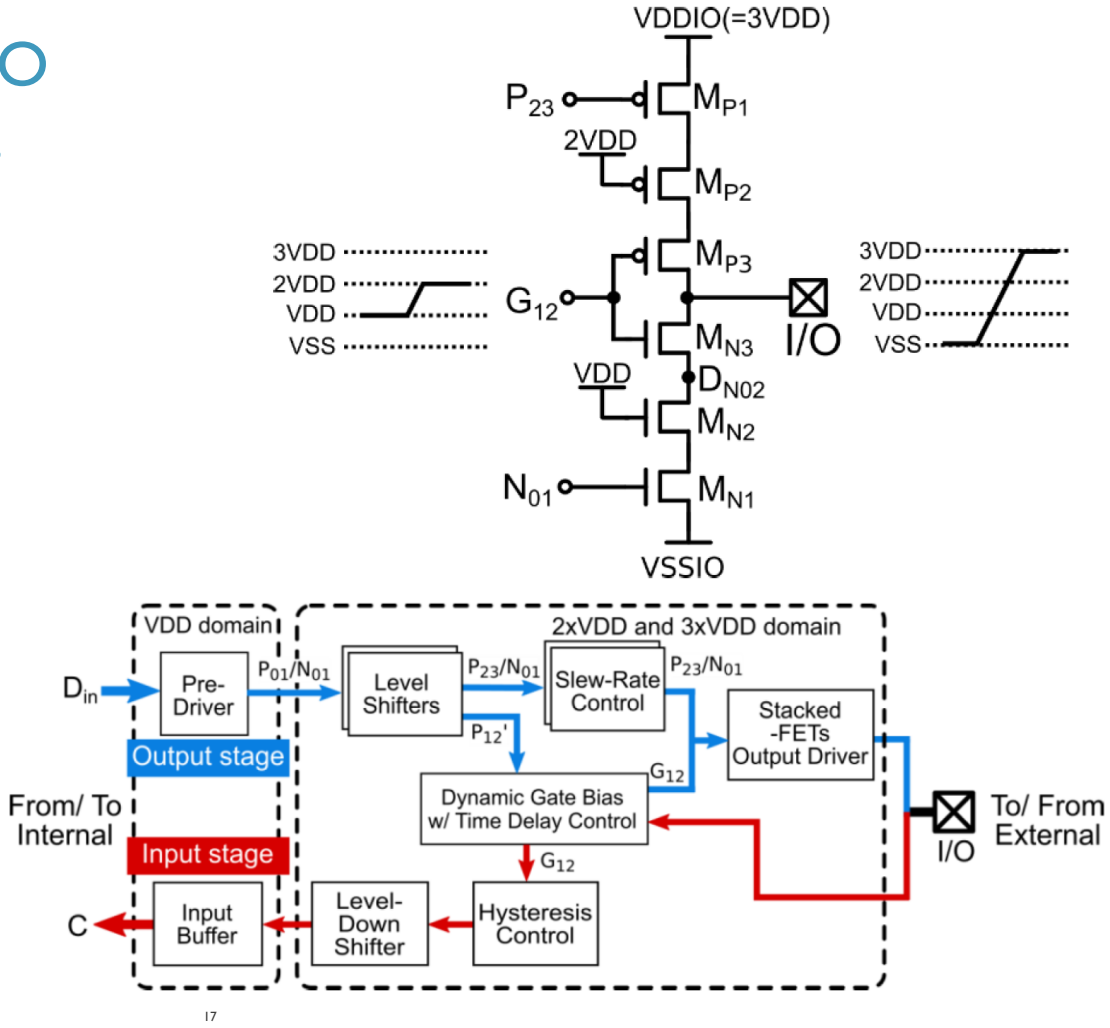
S.-H. Chen *et al.*, "vfTLP characteristics of ESD diodes in bulk si gate-all-around vertically stacked horizontal nanowire technology," in *2017 EOS/ESD Symposium*. doi: 10.23919/EOSESD.2017.8073454.

Left: K. Serbulova *et al.*, "Impact of Sub-µm Wafer Thinning on Latch-up Risk in STCO Scaling Era,", *EOS/ESD Symposium, 2021*. doi: 10.23919/EOS/ESD52038.2021.9574787. Right: W.-C. Chen et al., "ESD Challenges in 300nm Si Substrate of DTCO/STCO Scaling Options," *IEDM* 2023. doi: 10.1109/IEDM45741.2023.10413663.

3×VDD general-purpose I/O made with core transistors

- ~1.25x area penalty compared to thick-oxide equivalent (16nm FinFET) (this is w/o ESD layout)
- Including drain ballasting – no penalty!
- Dynamic bias needed to avoid overstress

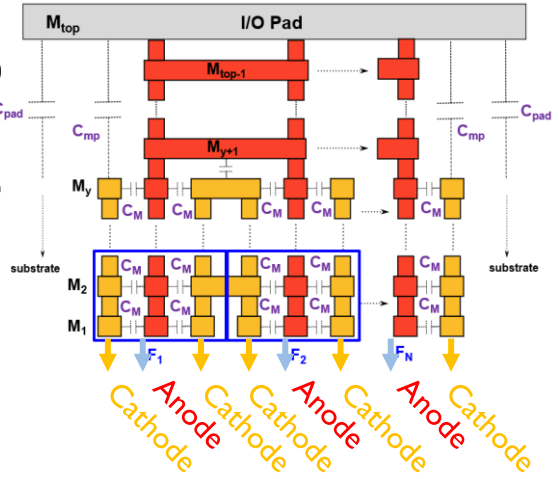
- GAA → no thick oxide, core I/O only solution



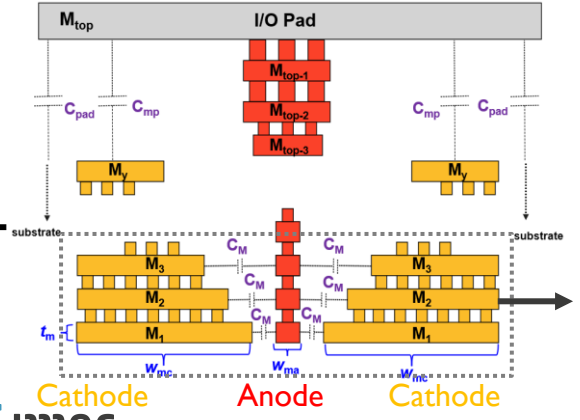
Wen-Chieh Chen et al., "A 1.8V GPIO with Design-Technology-Reliability Co-Optimization in Sub-3nm GAA-NS Technology", JSSC, 2024.

Tapered full-metal lines can improve both RF & ESD performance

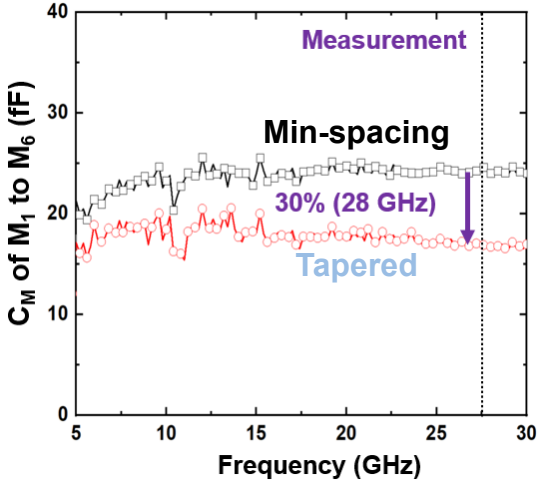
Min-spacing

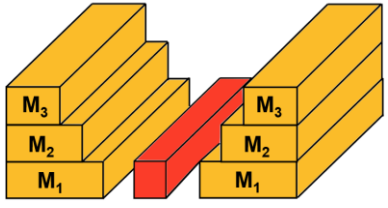


Tapered

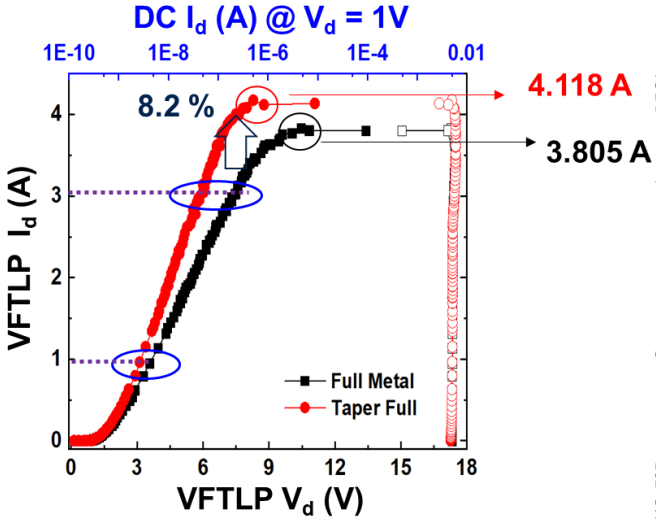


Better RF performance!





Improved VFTLP robustness!



Technology: 28nm CMOS
Target application: RF/High-Speed I/O

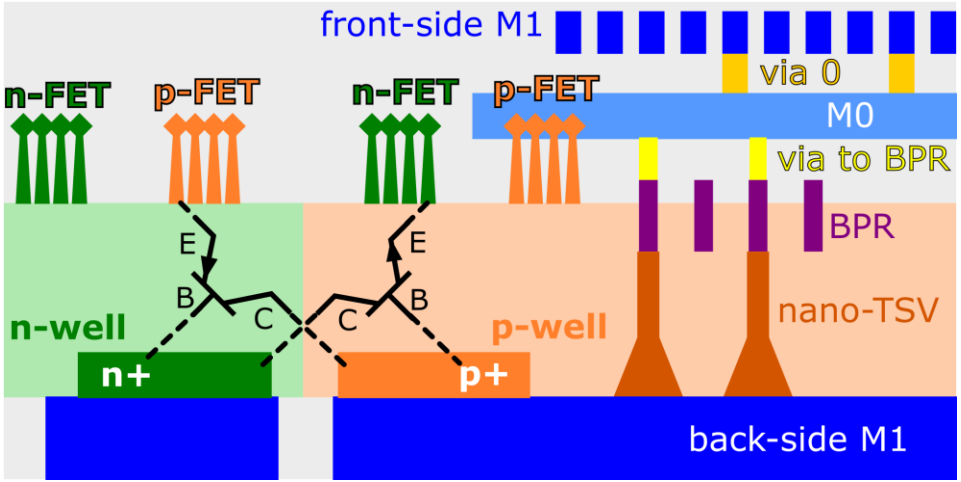
Wu, W.M. Et al., 2020. RF/high-speed I/O ESD protection: Co-optimizing strategy between BEOL capacitance and HBM immunity in advanced CMOS process. TED

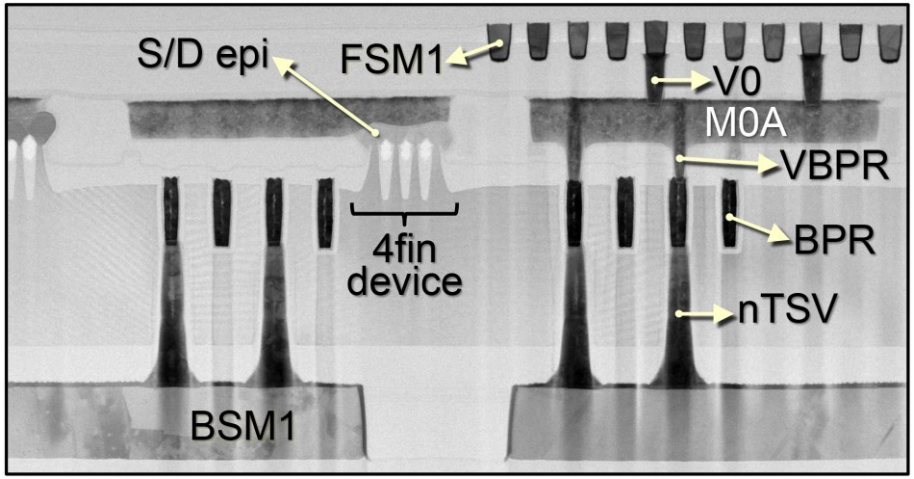
Wei-Min Wu, "Co-Optimization on RF/High-Speed I/O Pad: Efficient ESD Solution for 5G Heterogeneous Stacking Interface in Advanced CMOS Technology", international ESD Workshop 2021.

imec

Utilizing the chip backside

Backside contacts are very exciting option for ESD





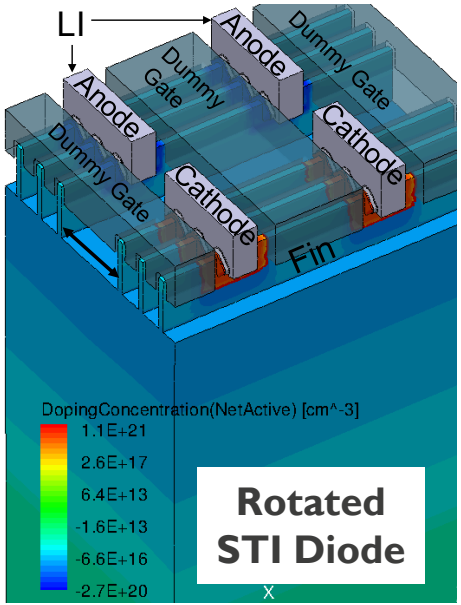
[A. Veloso, VLSI 2022]

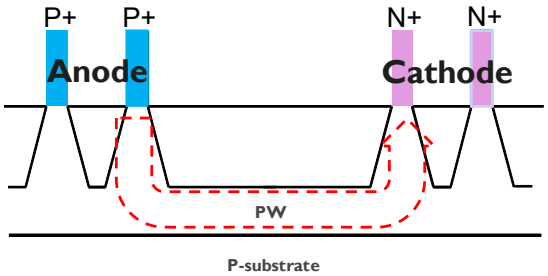
"The Transistor: An Indispensable ESD Protection Device – Part 2", InCompliance 2023, https://incompliancemag.com/the-transistor-an-indispensable-esd-protection-device-part-2/, accessed 18 August 2024.

imec

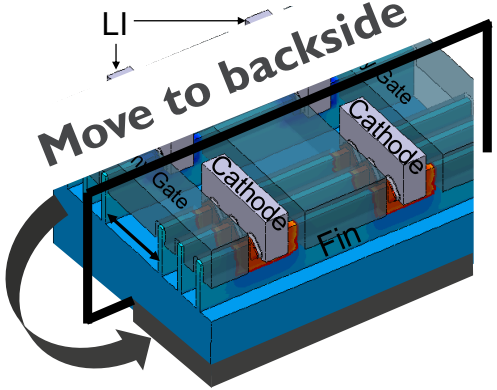
Vertical ESD diode

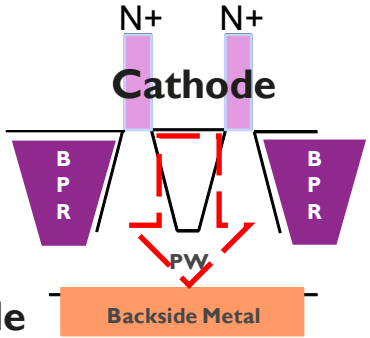
Traditional ESD diode





Vertical ESD diode

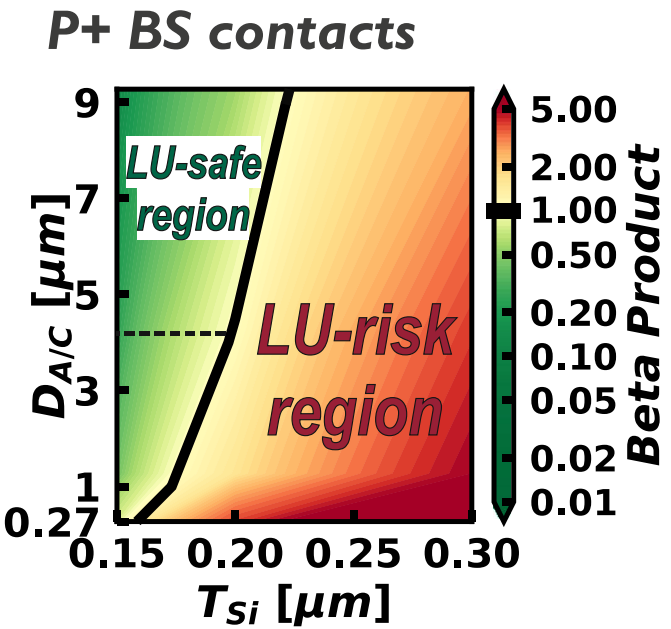


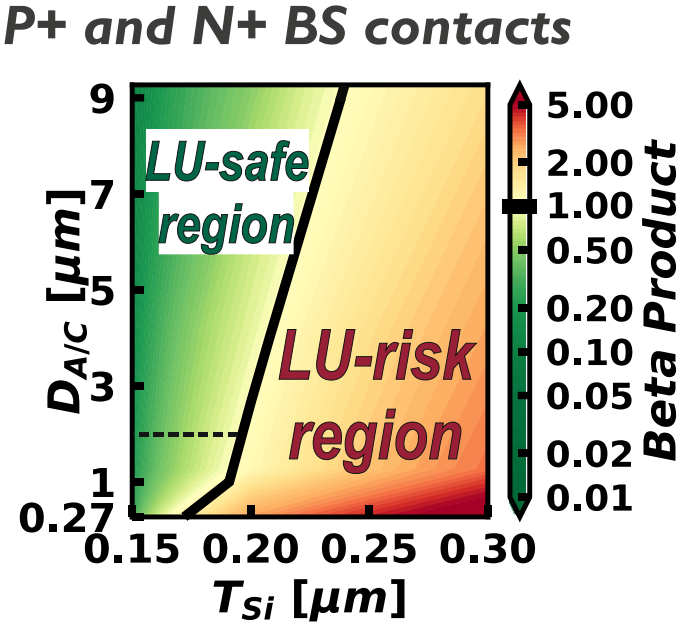


Proposed ESD diode: layout area reduces ~67% and It2/area increases 3x

Kateryna Serbulova et al. "Enabling Active Backside Technology for ESD and LU Reliability in DTCO/STCO." In 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)

Thin backside and backside implants reduce latch-up risk!



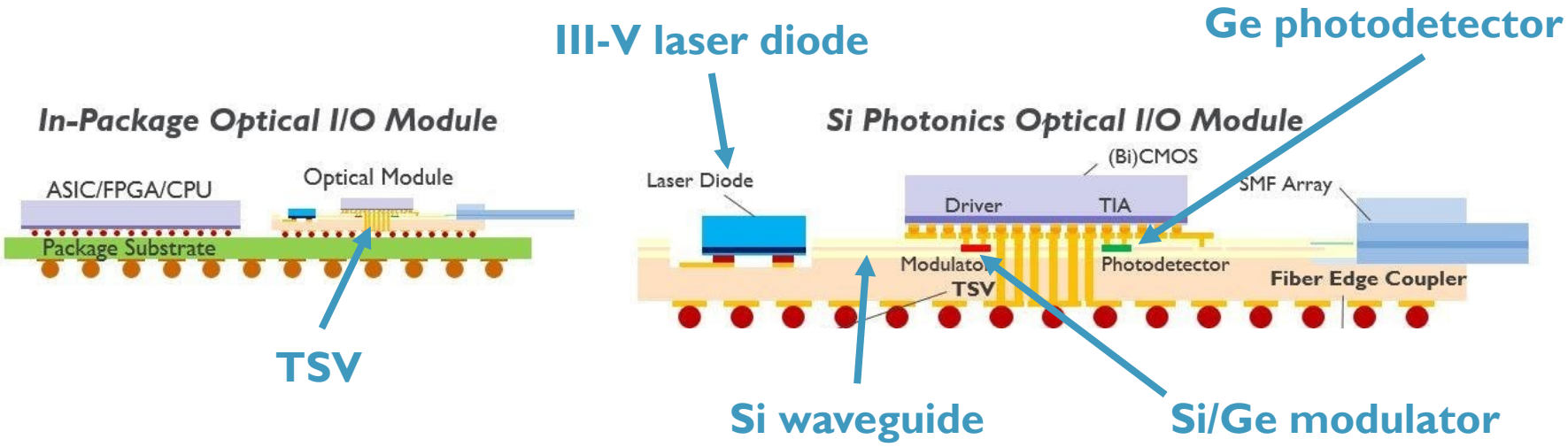


Kateryna Serbulova et al. "Enabling Active Backside Technology for ESD and LU Reliability in DTCO/STCO." In 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)

Optical I/O

No ESD from optical fibers, right?

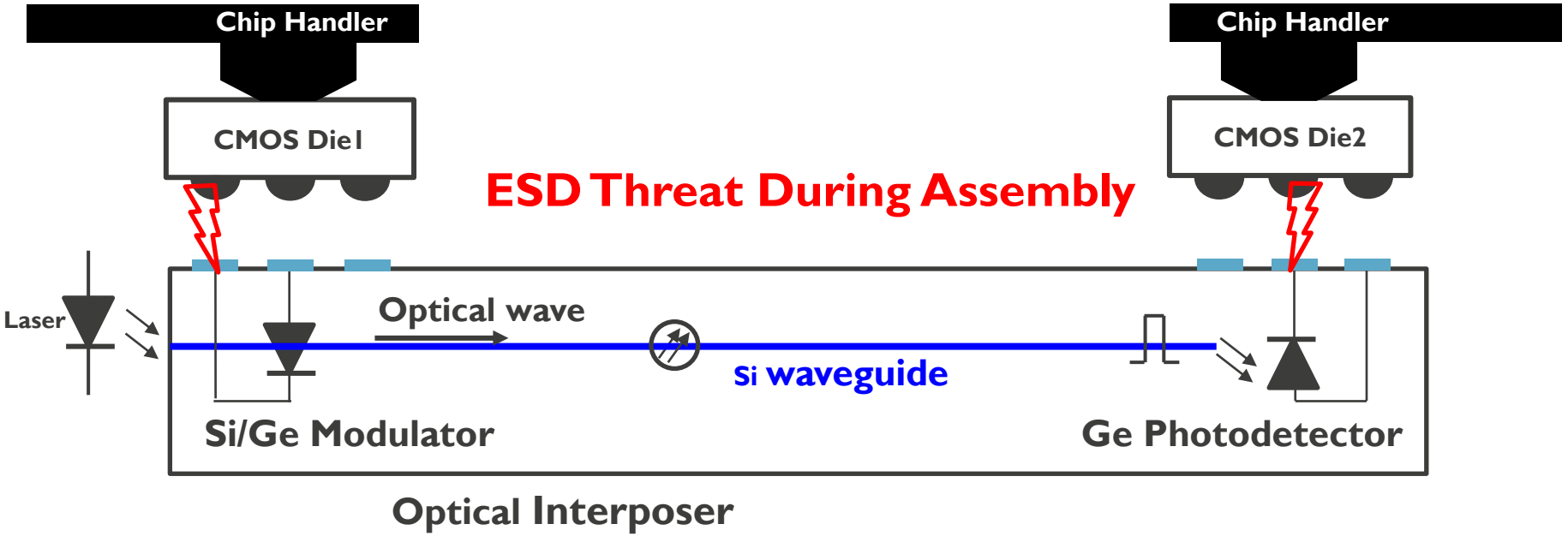
“External” communication with “internal” level of ESD protection



Perfect example of heterogeneous integration!

J. Bauwelinck, *et al*, *imec magazine*, 2018. - Silicon photonic interposers for 400Gb/s and beyond | imec (imec-int.com)

Optical diodes still need electrical power → ESD risk during assembly



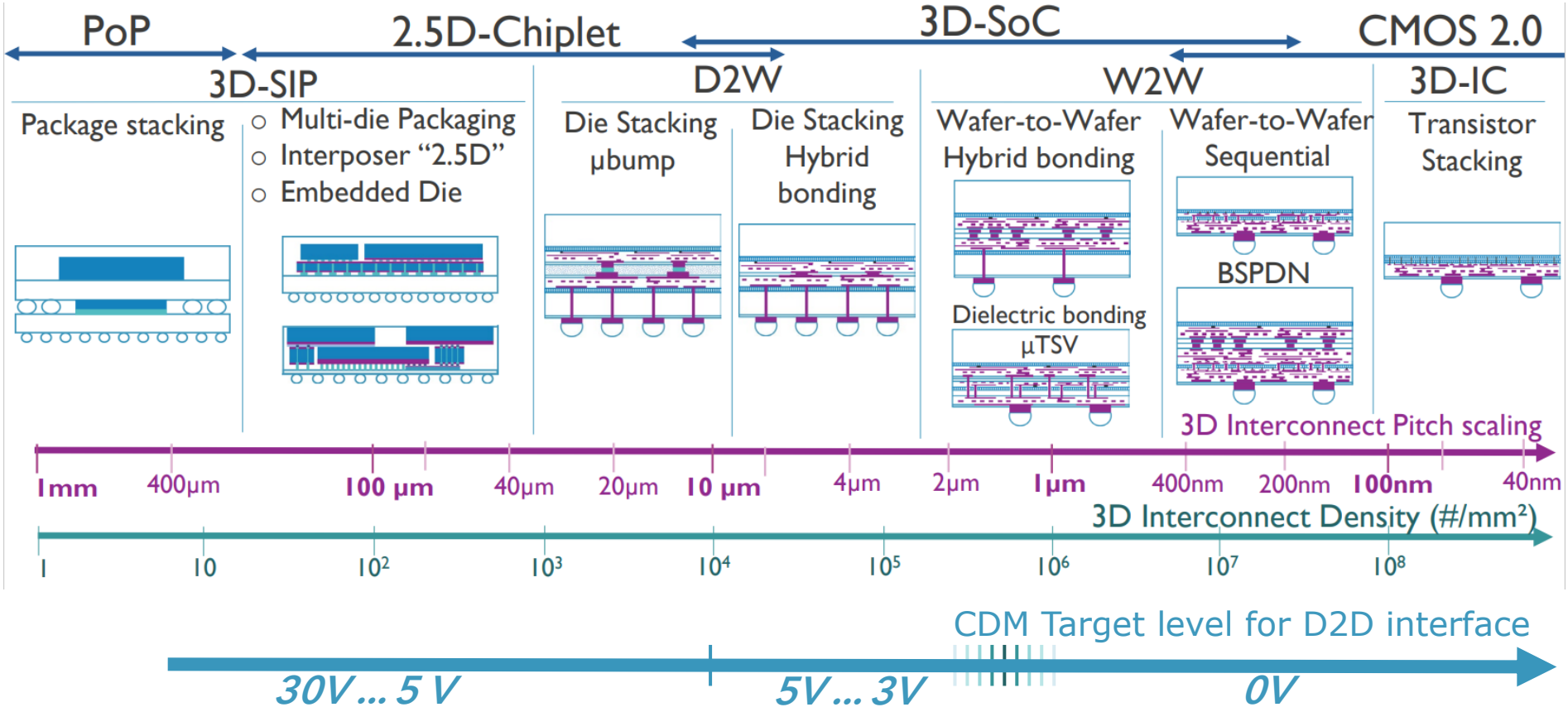
S.-H. Chen, K. Serbulova, et al., "ESD Robustness of Germanium Photodetectors in Advanced Silicon Photonics Technology", EOS/ESD Symposium 2024.

imec

Both OIO and backside connections need

2.5D and 3D interconnect

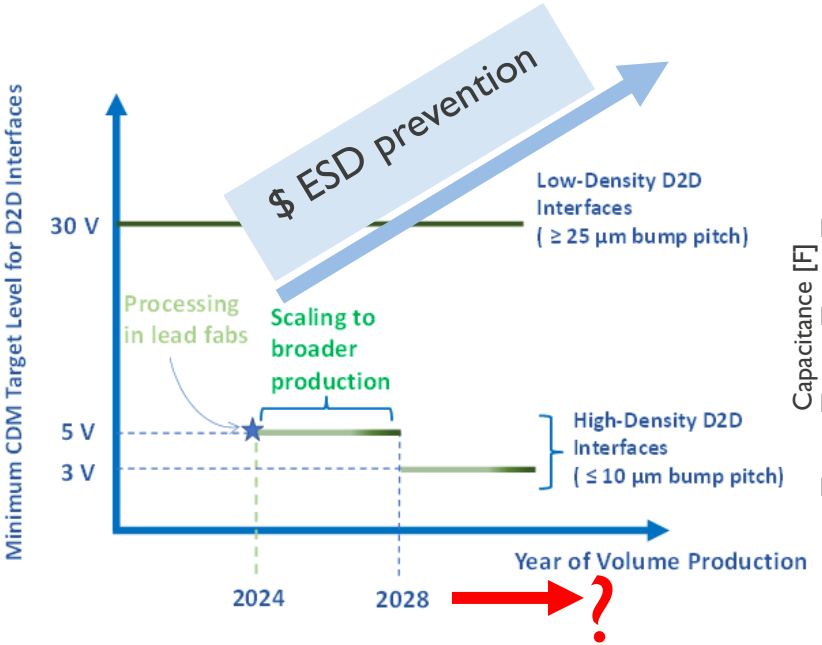
3D interconnect landscape + CDM ESD protection target voltages



[G. Van der Plas, E. Beyne, VLSI Circuits 2021.; S. Lin et al. VLSI Symposium 2024.; Industry Council on ESD Target Levels, "White Paper 2-2", 2023]

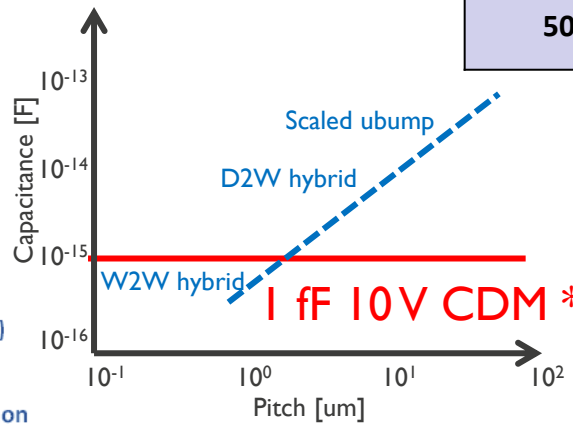
imec

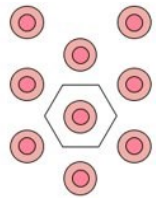
ESD protection of every signal pin will be difficult for W2W hybrid bonding, we need to investigate **ESD prevention** also!



[Industry Council on ESD Target Levels, "White Paper 2-2", 2023]

Pitch [nm]	Px	Py	Area [µm²]
1000	1075	931	1.00
500	537	465	0.25





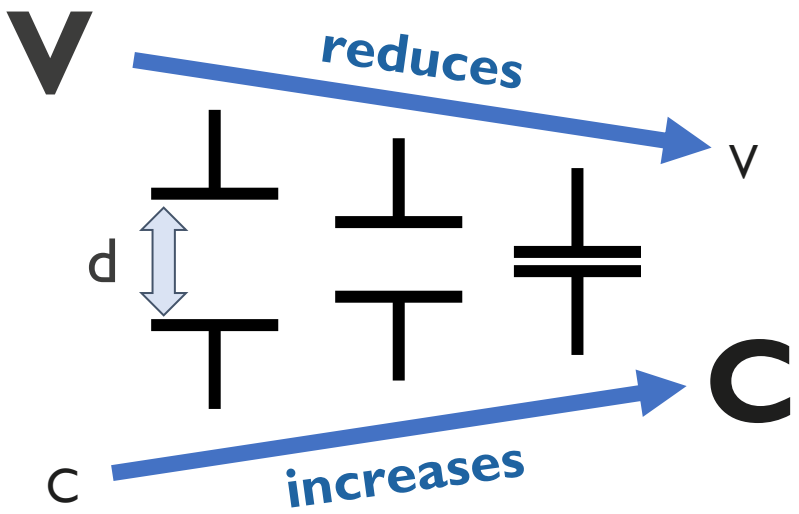
Area/pad

- The question is how do we meet 5V CDM targeted voltage for stacking technologies?
- Towards 0V CDM ?

* [Y-K. Chen IEDM2020]

imec

Voltage Suppression Lowers Voltage in Bonding

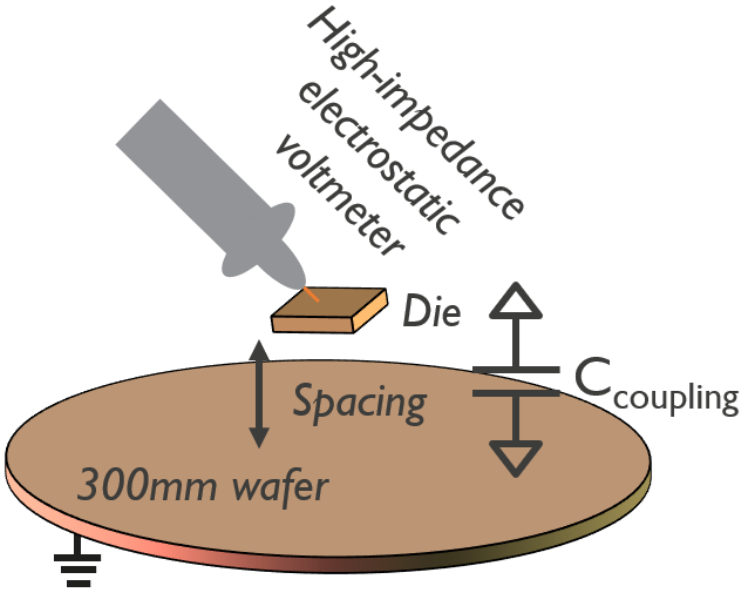


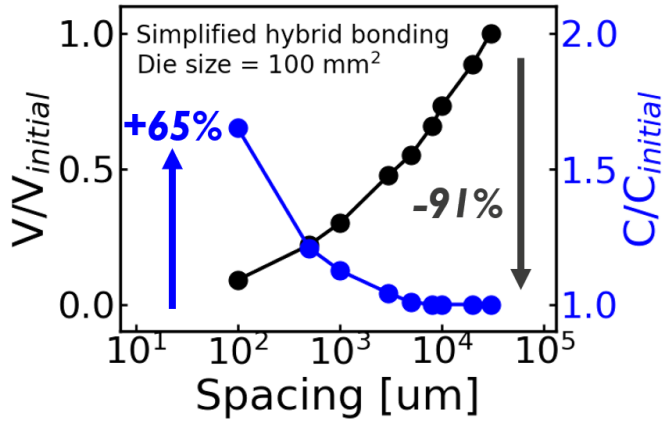
$$C = \frac{\varepsilon A}{d} \qquad Q = CV$$

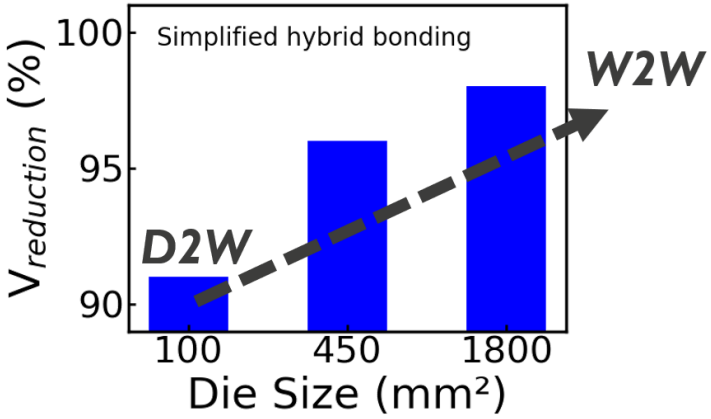
Voltage suppression effect:
W2W > D2W

A, Q, ε_0, ε_r → (constant) → A, Q, ε_0, ε_r

W2W Bonding shows Superior Voltage Suppression







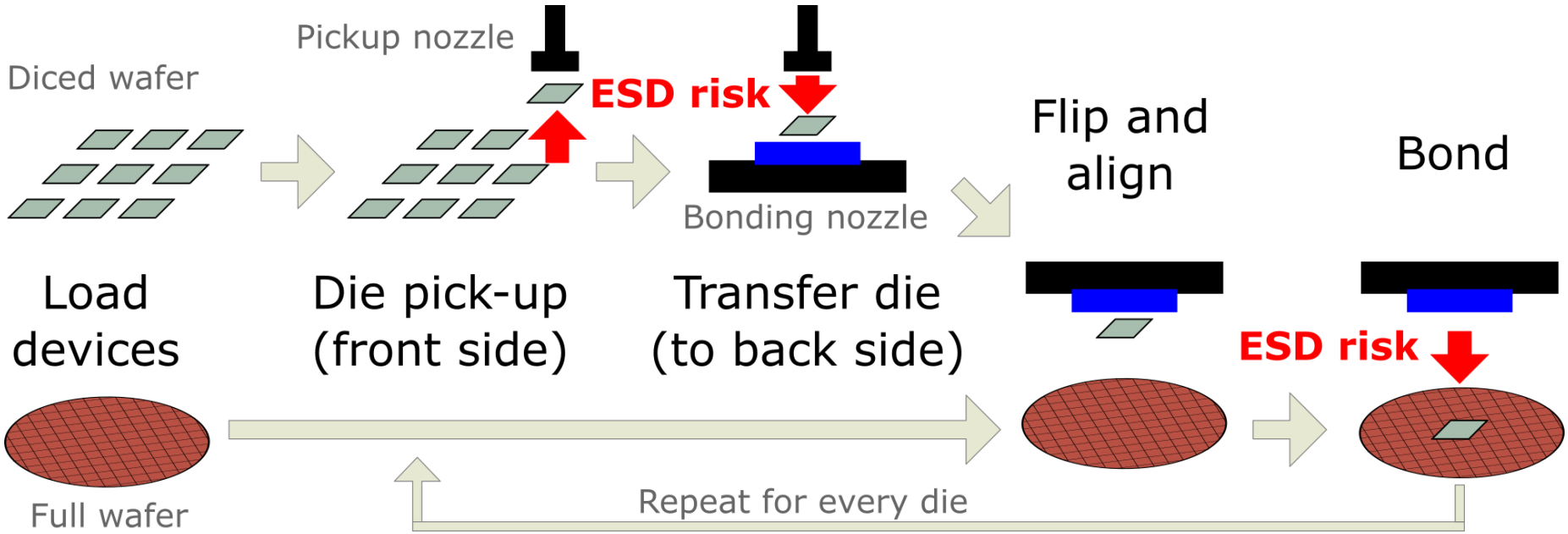
- D2W: ↑ 65% in $C_{coupling}$ and ↓ 91% in V
- Voltage suppression : W2W > D2W

[S. Lin et al. VLSI Symposium 2024]

imec

ESD control and bonding process assessment becomes more important than ever

Die-to-wafer (D2W) bonding process assessment



M. Simicic, F. Gibbon, S. Iacovo, S. H. Chen, G. Van der Plas, and B. Eric, "ESD process assessment of 2.5D and 3D bonding technologies," in *EOS/ESD Symposium Proceedings*, 2023.

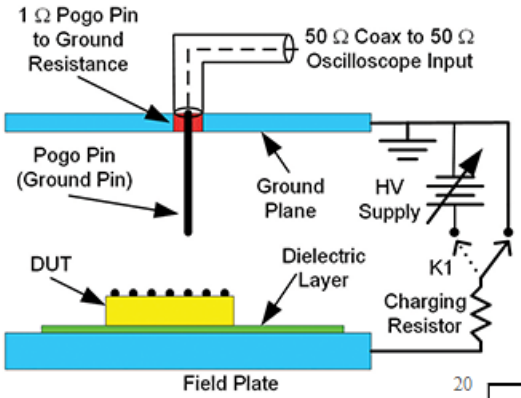
ESD control process assessment becomes essential in adv. bonding

- Installing an ionizer is not enough to guarantee 5V and 3V CDM
- Only way to guarantee ESD safety is customiyed prevention!

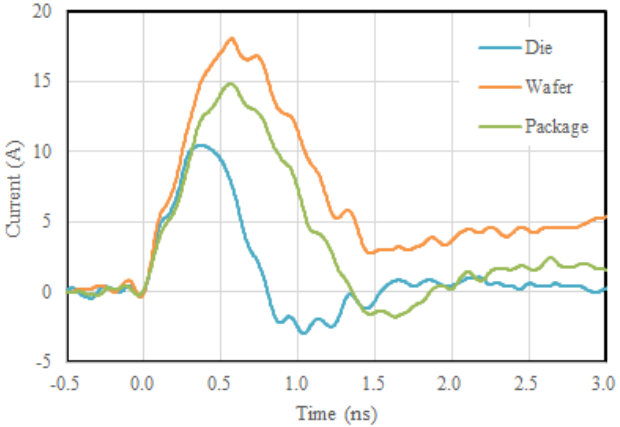
Testing ESD will change fundamentally

Shrinking bonding pads will make direct testing impossible

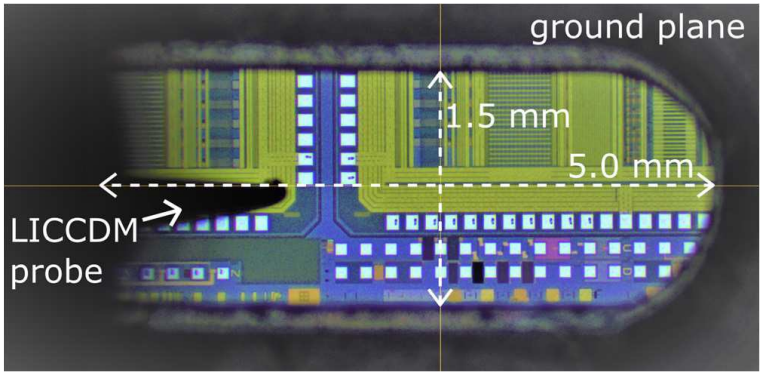
Field-induced-CDM (JS-002standard)
Package-level test

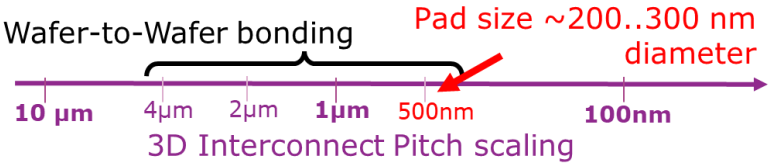


Sub-ns pulse width!



Contact CDM (no standard)
Bare die/wafer-level test





T. Suzuki et. al, EOS/ESD Symp. 2019.
M. Simicic et. al, EOS/ESD Symp. 2021.

Bringing it all together

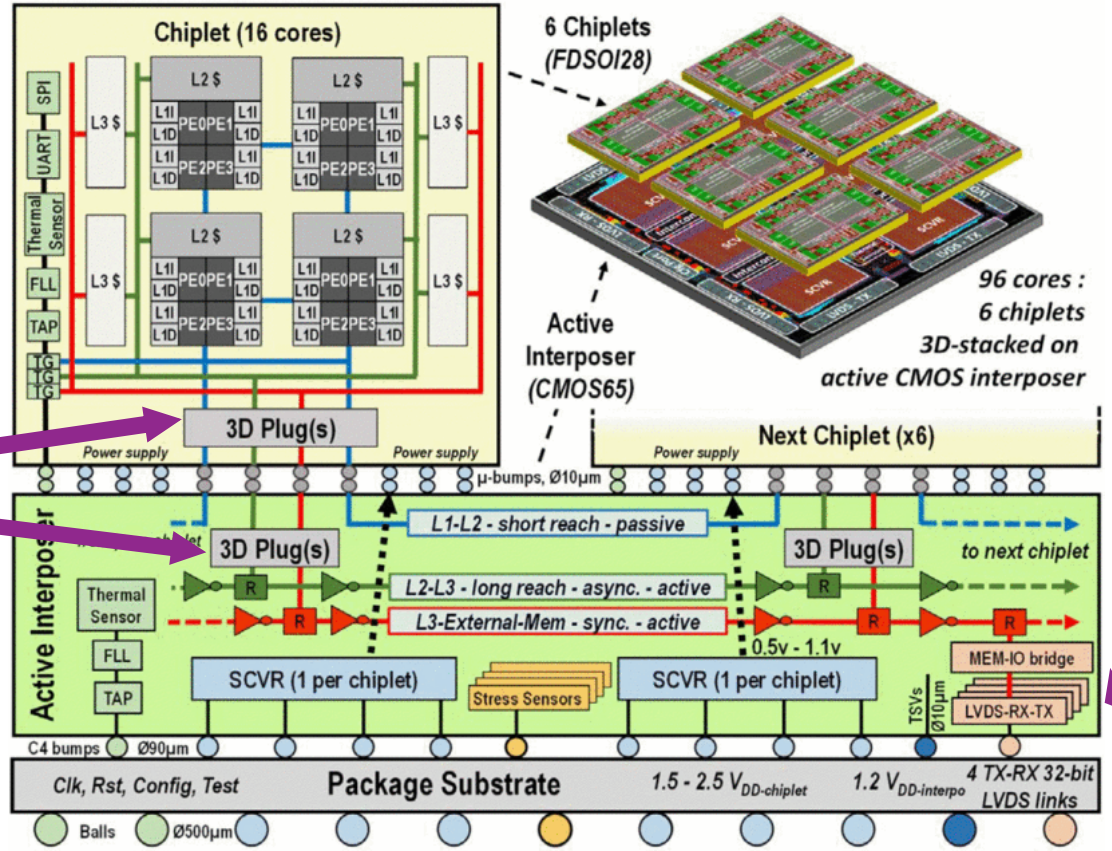
ESD protection moves from core chiplets to active interposers

28nm FDSOI core

I/O + ESD protection

65nm planar active interposer

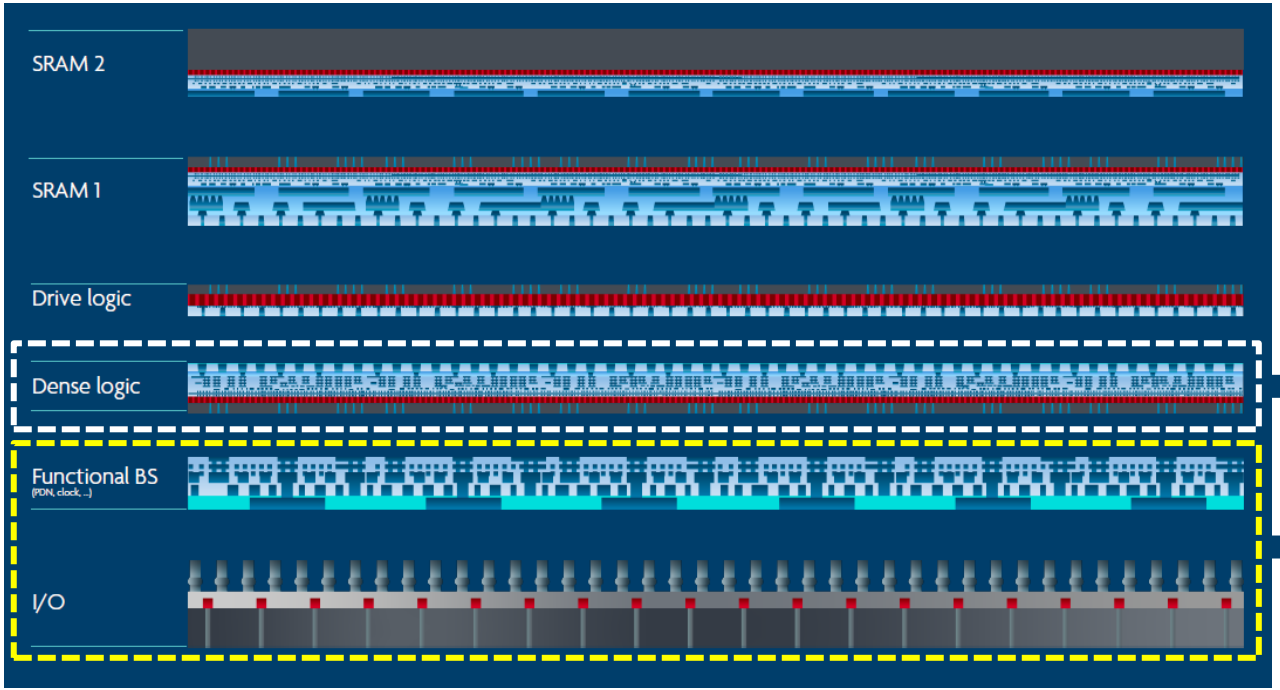
passive interposer



I/O + ESD

P. Vivet *et al.*, "2.3 A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm Latency, 3Tb/s/mm2 Inter-Chiplet Interconnects and 156mW/mm2@ 82%-Peak-Efficiency DC-DC Converters," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb. 2020, pp. 46–48. doi: 10.1109/ISSCC19947.2020.9062927.

It's all about rearchitecting towards a smart partitioning (CMOS 2.0)



Highest Cost
→ Will drive scaling

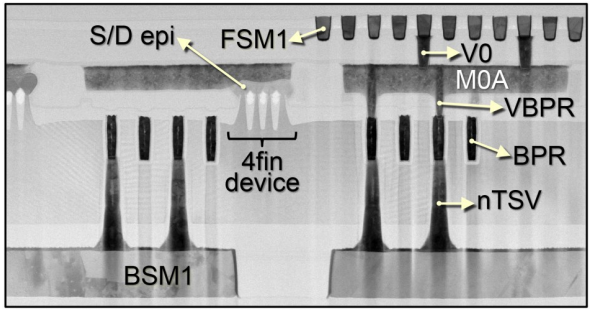
Lower Cost
→ ESD protection

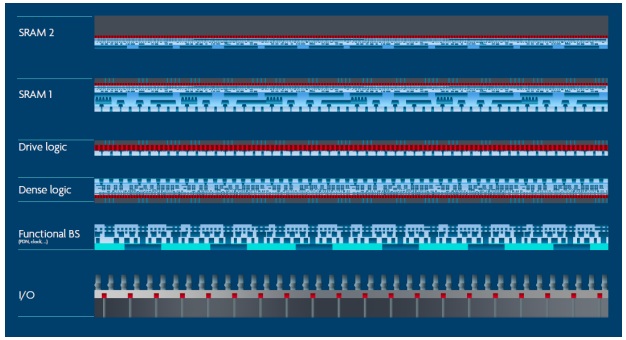
Same 'look & feel' as a classical CMOS platform

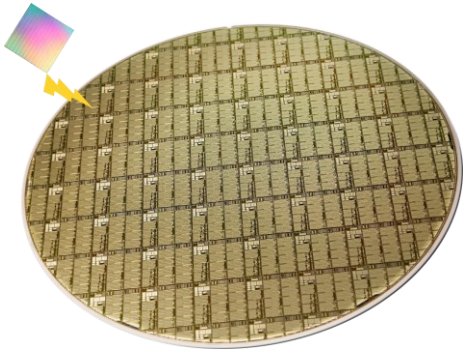
But offering versality for System optimization

J. Ryckaert and S. B. Samavedam, "The CMOS 2.0 revolution," *Nat Rev Electr Eng*, pp. 1–2, Jan. 2024, doi: 10.1038/s44287-023-00016-3.

Conclusions







- Si bulk is disappearing
- Creates opportunity for vertical diode

- Technologies become more function-specific
- ESD protection can move back to old tech.

- Reusability of chiplets is needed to reduce price
- Standardization is a must !

Acknowledgements

- Wen-Chieh Chen
- Wei-Min Wu
- Shih-Hsiang Lin
- Kateryna Serbulova
- Dimitri Linten
- Gregor Vercaigne
- Frank Gijbels
- Shih-Hung Chen
- Geert Van der Plas
- Eric Beyne
- Imec 3D program and partners
- Imec DTCO program and partners

YEARS

1984 - 2024

imec

HAPPY **INNO**VERSARY